ELECTRICALLY ERASABLE AND PROGRAMMABLE, NON-VOLATILE, SEMICONDUCTOR MEMORY DEVICE HAVING A SINGLE LAYER OF GATE MATERIAL, AND CORRESPONDING MEMORY PLANE

Abstract of the Disclosure

[0093] The semiconductor memory device includes an electrically erasable programmable non-volatile memory cell having a single layer of gate material and including a floating-gate transistor and a control gate. The source, drain and channel regions of the floating-gate transistor form the control gate. Moreover, the memory cell includes a dielectric zone lying between a first part of the layer of gate material and a first semiconductor active zone electrically isolated from a second active zone incorporating the control gate. This dielectric zone then forms a tunnel zone for transferring, during erasure of the cell, the charges stored in the floating gate to the first active zone.